WHAT IS CLAIMED IS:

1. A CCD pulse generator comprising:

digital delay type CCD control signal generating means for finely delaying a transfer signal for driving a CCD, thereby generating a plurality of delay signals, and changing selection of the plurality of delay signals, thereby generating a CCD control signal corresponding to set rise and fall timings;

turned-over/unturned-over signal generating means for generating a turned-over signal and an unturned-over signal of the CCD control signal;

selection means for selecting the turned-over signal and the unturned-over signal of the CCD control signal;

output means, having an output enable function, for outputting the signal selected by said selection means; and

output signal condition setting means for setting pieces of condition setting information that determine operations of said respective means.

2. A generator according to claim 1, wherein

the CCD pulse generator further comprises blanking means for temporarily disabling a CCD reset signal, and

the control signal includes the CCD reset signal.

3. A generator according to claim 1, wherein

the CCD pulse generator further comprises blanking means for temporarily disabling a CCD clamp signal, and

the control signal includes the CCD clamp signal.

4. A generator according to claim 1, wherein

the CCD pulse generator further comprises blanking means for temporarily disabling a CCD spare signal, and

the control signal includes the CCD spare signal.

5. A generator according to claim 1, wherein the control signal includes a CCD spare signal.

6. A generator according to claim 5, further comprising blanking means for temporarily disabling the CCD spare signal.

7. A CCD pulse generator comprising:

digital delay type sampling signal generating means for finely delaying a transfer signal for driving a CCD, thereby generating a plurality of delay signals, and changing selection of the plurality of delay signals, thereby generating a sampling signal for sampling a CCD output in synchronism with set rise and fall timings;

turned-over/unturned-over signal generating means for generating a turned-over signal and an unturned-over signal of a CCD control signal;

selection means for selecting the turned-over signal and the unturned-over signal of the CCD control signal;

output means, having an output enable function, for outputting the signal selected by said selection means; and

output signal condition setting means for setting pieces of condition setting information that determine operations of said respective means.

8. A generator according to claim 1, wherein said output signal condition setting means is formed by a

register which is controlled by three, data, clock, and load control signals.

9. A generator according to claim 8, wherein said output signal condition setting means is formed by a register which is controlled by three, data, clock, and load control signals, and can be cascade-connected to another functional element means formed by a register which is controlled by three, data, clock, and load control signals.

10. A generator according to claim 8, wherein the register is controlled via a terminal for selecting an element operation order.

11. A generator according to claim 8, wherein the register is controlled via a terminal for element enable selection.

12. A generator according to claim 8, wherein the register is controlled via communication by setting means including a CPU.

13. A generator according to claim 8, wherein said respective means are arranged in one chip of an integrated circuit.

14. A pulse generator unit which is formed by combining at least two of pulse generators defined in claims 2 to 6 and comprises a plurality of output means, wherein all output enable functions of said output means are simultaneously controlled by one setting.

15. A generator according to claim 1, wherein the

transfer signal is received by differential input means to generate the plurality of delay signals.

16. A generator according to claim 2, wherein

said respective means are arranged in one chip of an integrated circuit,

said blanking means comprises internal blanking signal generating means for generating a blanking signal within the integrated circuit, external blanking signal input means for receiving a blanking signal outside the integrated circuit, and blanking signal selection means for selecting the internal blanking signal and the external blanking signal, and

selection of said blanking signal selection means is set by said output signal condition setting means.

17. A generator according to claim 1, wherein a signal for driving a line CCD is generated.

18. An image forming apparatus comprising:

a CCD;

digital delay type CCD control signal generating means for finely delaying a transfer signal for driving said CCD, thereby generating a plurality of delay signals, and changing selection of the plurality of delay signals, thereby generating a CCD control signal corresponding to set rise and fall timings;

turned-over/unturned-over signal generating means for generating a turned-over signal and an unturned-over signal of the CCD control signal;

selection means for selecting the turned-over signal and the unturned-over signal of the CCD control signal;

output means, having an output enable function, for outputting the signal selected by said selection means; and

output signal condition setting means for setting pieces of condition setting information that determine operations of said respective means.

19. An apparatus according to claim 18, wherein

the image forming apparatus further comprises blanking means for temporarily disabling a CCD reset signal, and

the control signal includes the CCD reset signal.

20. An apparatus according to claim 18, wherein

the image forming apparatus further comprises blanking means for temporarily disabling a CCD clamp signal, and

the control signal includes the CCD clamp signal.

21. An apparatus according to claim 18, wherein

the image forming apparatus further comprises blanking means for temporarily disabling a CCD spare signal, and

the control signal includes the CCD spare signal.

22. An apparatus according to claim 18, wherein the control signal includes a CCD spare signal.

23. An apparatus according to claim 22, further comprising blanking means for temporarily disabling the CCD spare signal.